

Fig. 1

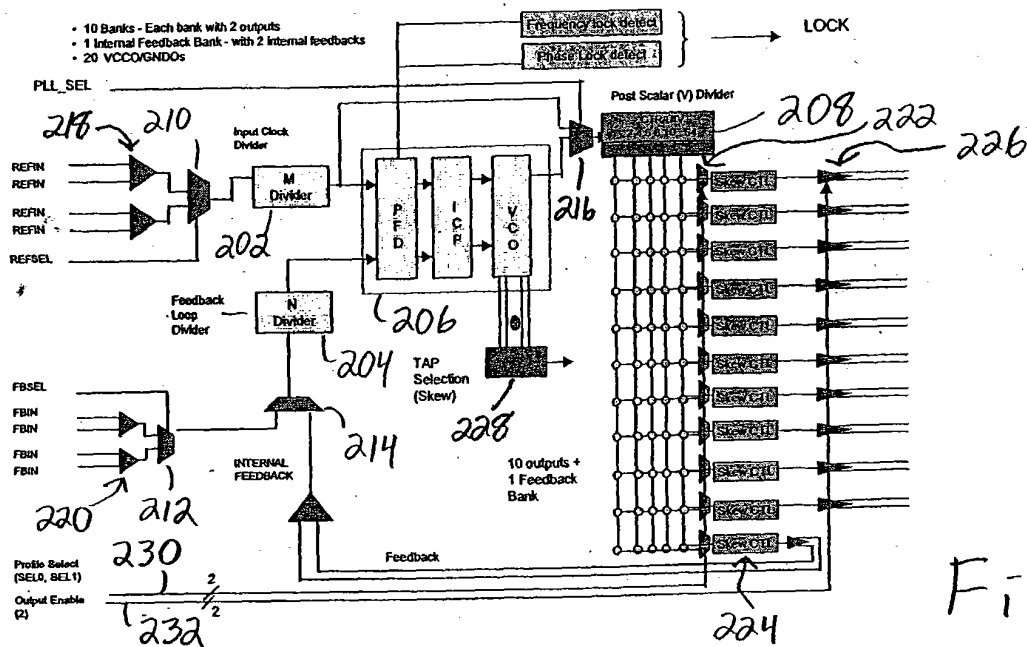


Fig. 2

External Frequency Select Control & Five Different Frequency Generations

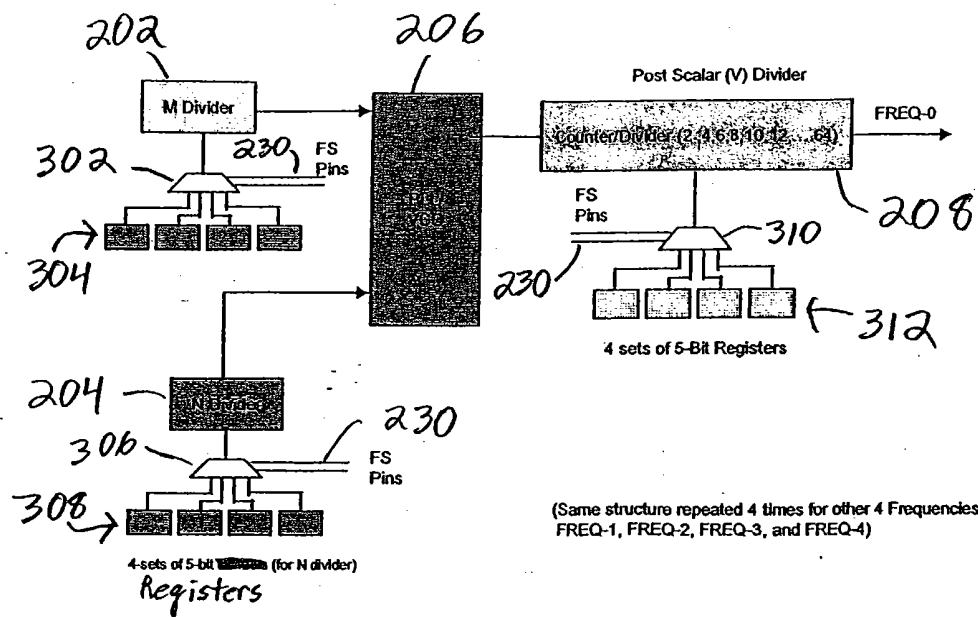


Fig. 3

External Frequency Select Control & Five Different Frequency Generations

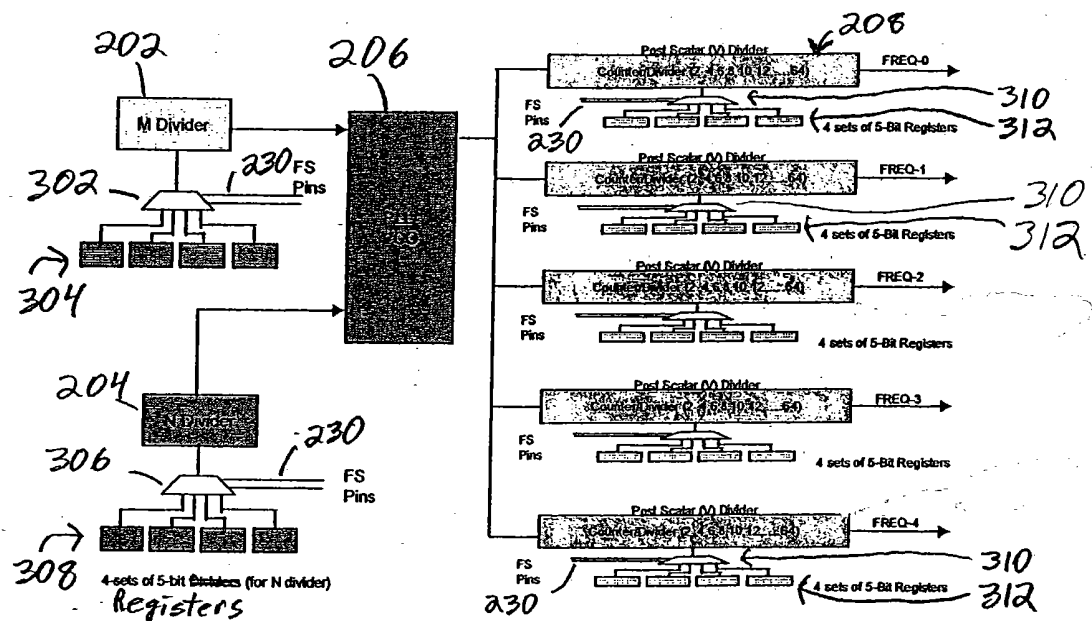


Fig. 4

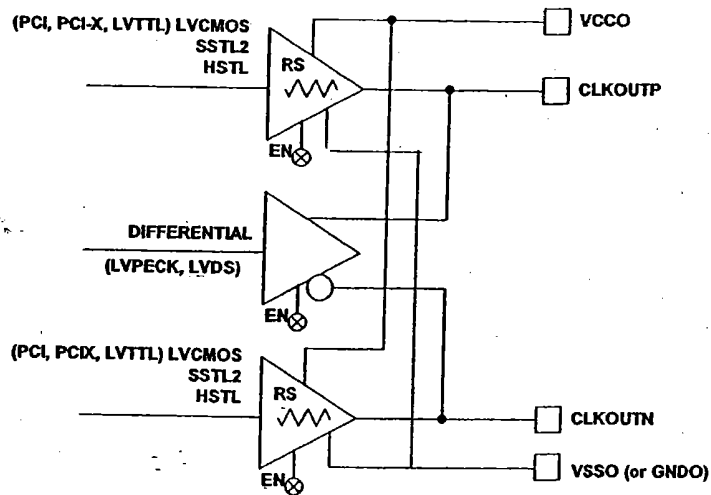


Fig. 5

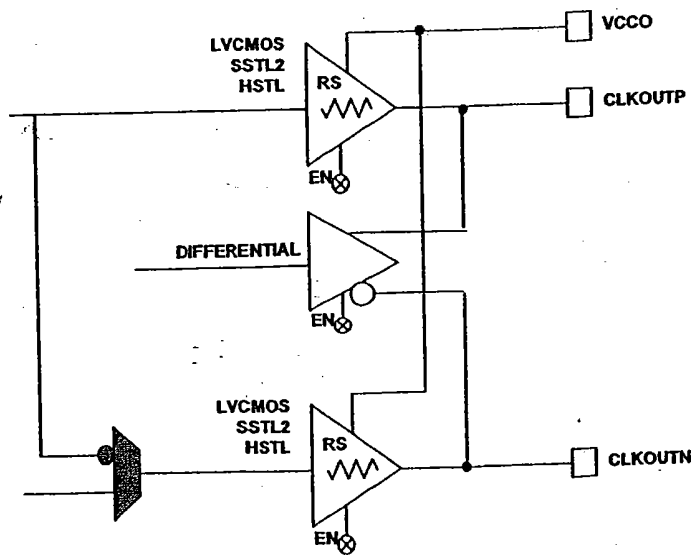


Fig. 6

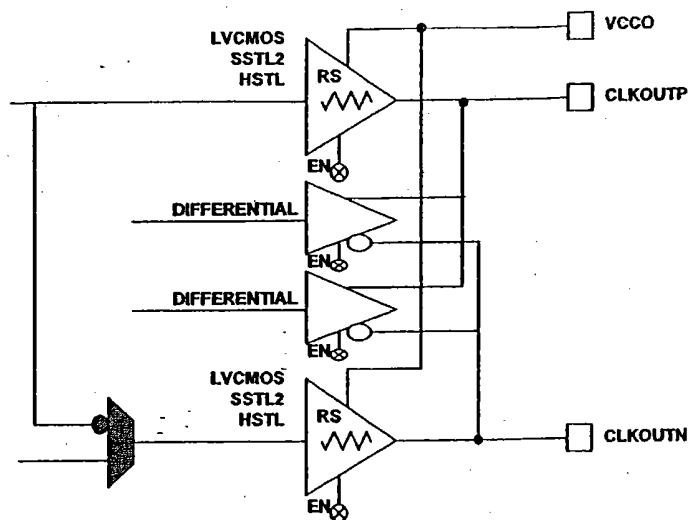
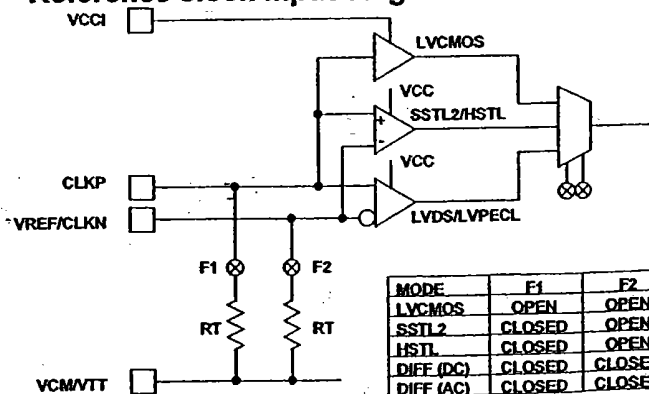


Fig. 7

Reference clock input stage



MODE	F1	F2	VREF/CLKN	VCM/VTT
LVC MOS	OPEN	OPEN	NC	NC
SSTL2	CLOSED	OPEN	1.25V	VTT(1.25V)
HSTL	CLOSED	OPEN	0.75V	VTT(0.75V)
DIFF (DC)	CLOSED	CLOSED	CLKN	OPTIONAL
DIFF (AC)	CLOSED	CLOSED	CLKN	VCM

800

Fig. 8

SSTL2/HSTL input application

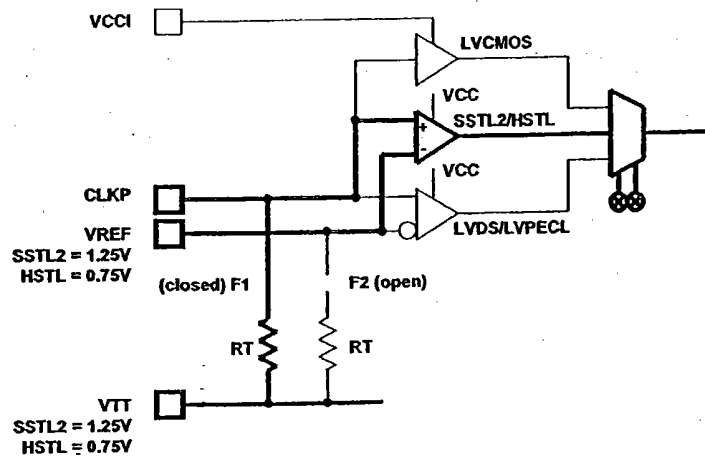


Fig. 9

Alternative DC coupled differential application

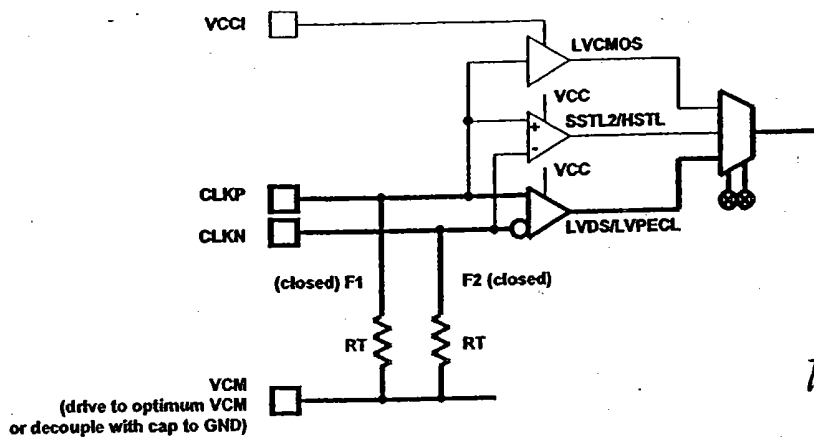
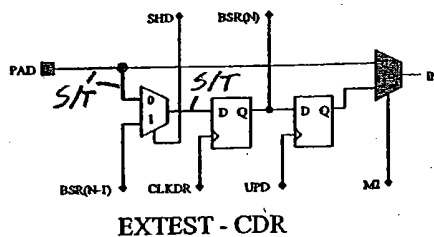


Fig. 10



Input Boundary Scan Cell

Fig. 11

1100

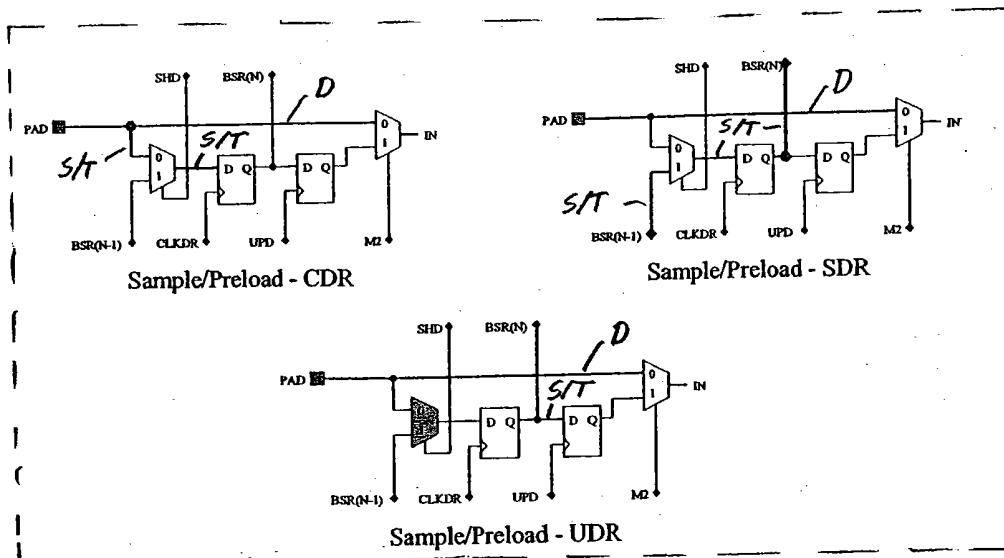


Fig. 12 - Sample/Preload BSC Operation

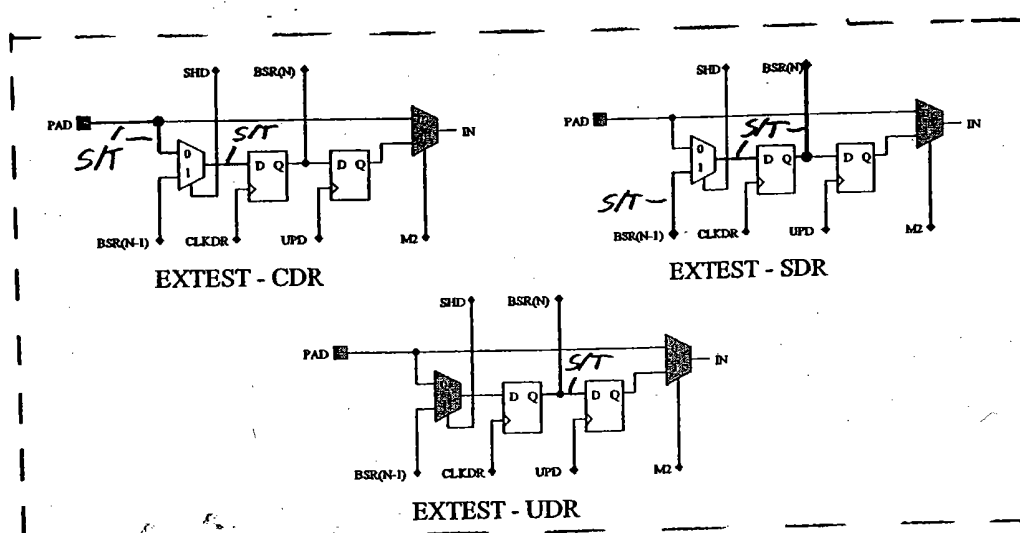


Fig. 13 - EXTEST BSC Operation

